PATENT
P54766

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

1721

In re Application of:

Geun-Woo PARK

Serial No.:	08/922,300	Examiner:	M. Marc-Coleman
Filed:	2 September 1997	Art Unit:	3661

For: DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

Appeal No._____

The Honorable Commissioner
of Patents & Trademarks
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S REPLY BRIEF (37 CFR §1.192)

In response to the Examiner's Answer (Paper No. 20), mailed 17 September 2001, entry and consideration of this reply brief is respectfully requested.

This reply brief is transmitted in triplicate (37 CFR §1.192(a)).

REPLY BRIEF

I. STATEMENT OF REAL PARTY IN INTEREST

Pursuant to 37 CFR §1.192(c)(1) the real party in interest is:

SamSung Electronics Co., Ltd.
416 Maetan-dong, Paldal-ku,
Suwon City, Kyungki-do,
Republic of Korea

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 CFR §1.192(c)(2), there are no appeals nor interferences known to the Appellant, the Appellant's legal representative, or the Assignee (real party of interest) which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The Examiner errs in stating that the Appeal Brief does not contain the foregoing statement.

III. STATUS OF CLAIMS

Claims 1-11 have been finally rejected and are appealed herein.

IV. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendment has been filed after receipt of the final rejection (Paper No. 17).

V. SUMMARY OF THE INVENTION

Page 10, line 5 - Page 13, line 11

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a power interruption delay function in accordance with the present invention. In the display device of Fig. 3, the voltage source V1 is connected to the input terminal of the H/V processor constant voltage circuit 131 through the power interruption delay charging circuit 370.

The power interruption delay charging circuit 370 includes a reverse voltage prevention diode D1 having its anode connected to the voltage source V1 and its cathode connected to the input terminal of the H/V processor constant voltage circuit 131, and a polarity capacitor C1 having its positive pole connected to a connection point of the cathode of the reverse voltage prevention diode D1 and the input terminal of the H/V processor constant voltage circuit 131 and its negative pole connected to the ground voltage terminal.

The operation of the display device with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail.

When the display device is powered on, the high voltage from the high voltage source B+ is charged on the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 and then discharged through the discharge loop including the horizontal output transistor TR in the horizontal output circuit 134. Such charging and discharging operations are repeated as stated previously with reference to Fig. 2.

If the power supply to the display device is interrupted during the operation of the display

device, the voltage supply to the H/V processor constant voltage circuit 131 is at once stopped in the display device of Fig. 2, as shown in Fig. 4a. However, according to the present invention, a voltage, charged on the polarity capacitor C1 during the power supply, is applied to the input terminal of the H/V processor constant voltage circuit 131, as shown in Fig. 4b, while it is discharged. As a result, the H/V processor constant voltage circuit 131 does not immediately stop the voltage supply to the H/V processor 132.

Noticeably, the reverse voltage prevention diode D1 is connected in series between the voltage source V1 and the H/V processor constant voltage circuit 131 to protect the power supply circuit by allowing the voltage charged on the polarity capacitor C1 not to be discharged to the voltage source V1 at the power interruption state.

Because the voltage charged on the polarity capacitor C1 is continuously applied to the H/V processor constant voltage circuit 131 until it is completely discharged, the voltage supply to the H/V processor 132 is not interrupted immediately. Therefore, the H/V processor 132 outputs the horizontal pulse signal continuously for a predetermined time period, as shown in Fig. 5b.

The continuous pulse output time of the H/V processor 132 is determined according to a discharge time of the polarity capacitor C1. As a result, the continuous pulse output time of the H/V processor 132 can be varied by adjusting the discharge time of the polarity capacitor C1.

While the output pulse from the H/V processor 132 maintains such a high voltage level as to continuously drive the field effect transistor FET2 in the horizontal driver 133, the horizontal drive transformer T2 continues to be excited to induce a voltage in its secondary coil, thereby causing the horizontal output transistor TR in the horizontal output circuit 134 to remain at its driven

state. Hence, the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs can be sufficiently discharged. Namely, the discharge time of the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs is sufficient.

As apparent from the above description, according to the present invention, the power interruption delay charging circuit is provided at the input terminal of the H/V processor constant voltage circuit in the display device. The power interruption delay charging circuit can prevent the horizontal output transistor from being damaged due to an instantaneous surge current when power supply is resumed after power interruption. Further, the power interruption delay charging circuit can prevent the peripheral devices and circuits from being successively damaged due to damage in the horizontal output transistor.

VI. ISSUES

Whether claims 1-11 are patentable under 35 U.S.C. §103(a) over Applicant's admitted prior art in view of Van Clifton.

VII. GROUPING OF CLAIMS

Claim 1 stands or falls alone, and claims 2-11 stand or fall with claim 1.

The Examiner errs in stating that the Appeal Brief does not contain the foregoing grouping.

VIII. ARGUMENT

Claims 1-11 are not obvious and unpatentable under 35 U.S.C. §103(a) in view of the

combined teachings of Applicant's admitted prior art and Van Clifton Martin '348 (*hereafter:* Martin). The Applicant respectfully traverses this rejection for the following reason(s).

Since the patentability of all the claims depend upon the patentability of claim 1, then only the limitations of claim 1 need be addressed.

With respect to claim 1, Applicant's admitted prior art teaches all that is claimed except the feature of *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted,* which is deemed to be non-obvious in view of the proposed combination of art.

The Examiner agrees with the foregoing; see the Examiner's Answer, page 10, paragraph 11.

The Examiner applied Martin in an erroneous attempt to obviate the claims. The Examiner refers us to col. 2, lines 64-72, which state:

> The control grid 14 is clamped to a negative DC bias voltage -V1 from the power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed.

Although Martin fails to teach or suggest, to one of ordinary skill in the art, gradually lowering the input voltage to a H/V processor constant voltage circuit when power supplied to the display device is interrupted, the Examiner appears to utilize a portion of the gist of the invention,

i.e., a power interruption delay function, in combination with Martin's "protection circuit for the **screen** of a cathode ray tube." Note here, however, that Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen.

The present invention is directed toward a display device with a power interruption delay function, in which a power interruption delay charging circuit is provided **to prevent a horizontal output transistor from being damaged** due to an instantaneous surge current generated when power supply is resumed under the condition that a high voltage charged on a horizontal deflection coil and an S-correction capacitor is not sufficiently discharged after power interruption.
A rejection based on the gist of the invention is contrary to case law. *See Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.* 796 F.2d 443, 230 USPQ 416 (Fed. Cir. 1986).

Additionally, the Examiner erroneously holds that Martin's diode 44 and capacitor 45 have the same function as the Appellant's circuitry. It can be seen in the Examiner's Answer, paragraph 11, page 11 the Examiner emphasizes the phrase "drop slowly" with regard to Martin's teaching of gradually or slowly lowering the DC input voltage to the control grid of a screen. Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen. Although the function of diode 44 and capacitor 45 is to make the voltage at the control grid 14 drop slowly, that is an entirely different function from the Appellant's power interruption delay charging means which gradually lowers the input voltage to the H/V processor constant voltage circuit when power supplied to the display device is interrupted. In the Appellant's invention, **a horizontal output transistor** TR in the horizontal output circuit 134 (Fig. 3) is protected. Martin **does not** teach that diode 44 and

cathode 45 function to **protect** anything.

Accordingly, Martin's diode 44 and capacitor 45 clearly does not perform the same function as the Appellant's circuitry. The Examiner clearly errs in this regard.

Further, the Examiner errs in stating that one of ordinary skill in the art "can easily [come] up with the Applicant's invention," when considering Applicant's admitted prior art together with Martin. The Appellant disagrees. Instead Martin would have suggested **only** what Martin teaches, *i.e.,* clamping a control grid (not shown) of the monitor of Applicant's admitted prior art to a negative DC bias voltage -V1 from a power supply by a diode connected between voltage -V1 and the control grid and a capacitor connected between the control grid and ground.

Looking closer at what Martin **actually** teaches, Martin notes a problem that a power loss could result in a **high beam current** and local overheating of the screen, called phosphor or screen burn spots. See col. 1, lines 15-20. Martin provides three parallel protection circuits (34, 35 and 36) to prevent screen burn spots: 1) protection circuit 34 is a cathode control circuit that will inhibit the beam current by controlling the voltage produced by unblank driver 22 for cathode 13; 2) protection circuit 35 is an accelerator grid control circuit that functions to short any voltage at accelerator grid 15 to ground; and 3) protection circuit 36 is a horizontal deflection control circuit that horizontally deflects the beam off the screen while the voltage at accelerator grid 15 is decaying to zero.

1) Cathode control circuit 34 includes an AND gate 42 that prevents beam generation when protection is required. Martin **does not** teach that diode 44 and cathode 45 function

to **protect** the screen or any other protection function.

2) Accelerator grid control circuit 35 is necessary to short accelerator grid 15 to ground because the capacitance in capacitor 46 would normally prevent an immediate drop to zero.

3) Horizontal deflection control circuit 36 includes a transistor 58, resistors 61 and 62, relay coil 65, and relay contact 64. To prevent screen burn spots, transistor 58 is turned on by the two bias voltages provided via resistors 61 or 62. These two bias voltages are arranged so that if one fails the other will be present. Also, the value of these bias voltages are chosen so that even if there is a power failure, the voltages decay off at a slow enough rate so that transistor 58 will be turned on long enough to cause the beam to be horizontally deflected off the screen, thereby preventing the beam from burning the screen.

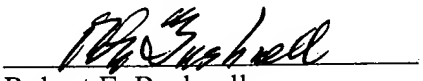
It might have been obvious to replace Martin's resistors 61 and 62 with a diode-capacitor network similar to diode 44 and capacitor 45 in Martin, in order to gradually lower the bias voltage to transistor 58, however, transistor 58 is not equivalent to H/V processor constant voltage circuit 131 utilized by the Admitted prior art of Appellant's Fig. 2. Not one of the three protection circuits, nor any other teaching found in Martin, would have motivated one of ordinary skill in the art to modify the Admitted prior art of Appellant's Fig. 2 in order to gradually lower the input voltage to the H/V processor constant voltage circuit 131 when power supplied to the display device is interrupted. Note, for example X drive 99 in Fig. 2 of Martin is an AC voltage source which provides a voltage to horizontal deflection circuit 23 in Martin; Martin does not suggest gradually lowering the input voltage to X drive 99 if a power failure occurs.

Therefore, a display device derived from the combined teachings of Applicant's admitted prior art and Martin fails to teach a *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.* The claim must be considered on the whole without omitting critical elements or steps of the invention.

Therefore claim 1 is not obvious in view of the applied art.

Accordingly, the rejection of claims 1-11 is deemed to be in error and should not be sustained.

Respectfully submitted,



Robert E. Bushnell
Attorney for Applicant
Reg. No.: 27,774

Suite 300, 1522 K Street, N.W.
Washington, D.C. 20005
(202) 638-5740

Folio: P54766
Date: 11/13/01
I.D.: REB/MDP

IX. APPENDIX

CLAIMS UNDER APPEAL

1. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a current amplifier for amplifying current in response to the pulse width modulation signal from said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

2. The display device as set forth in claim 1, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

3. A display device with a power interruption delay function, comprising:

a power supply circuit for converting a received commercial AC power into a DC input voltage;

a horizontal deflection circuit under the control of a microcomputer, receiving said DC input voltage, for horizontally deflecting electron beams generated in said display device; and

power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:

a polarity capacitor for performing a charging operation when said AC power

is supplied and a discharging operation when said AC power is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted.

4. The display device as set forth in claim 3, wherein said horizontal deflection circuit comprises:

a pulse width modulation controller for generating a pulse width modulation signal under the control of said microcomputer;

a current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting said electron beams;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver; and

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to said DC input voltage, said DC input voltage being received through said power interruption delay charging means.

5. The display device as set forth in claim 4, wherein said current amplifier comprises:

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor FET1 having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to said ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal.

6. The display device as set forth in claim 5, wherein said horizontal output circuit

comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

7. The display device as set forth in claim 6, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.

8. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to a ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection

coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

9. The display device as set forth in claim 8, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

10. The display device as set forth in claim 8, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

11. The display device as set forth in claim 10, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.